REMARKS

The Examiner is thanked for re-opening prosecution of this application in response to the Appeal Brief filed January 21, 2010.

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Rejections under 35 U.S.C. §102(b) and §103(a)

With respect to the rejection of claims 1 and 3 under 35 U.S.C. §102(e) as being anticipated by Dupenloup (US 6,289,498), and with respect to the 35 U.S.C. §103(a) rejection of claims 2 and 4-5 as being unpatentable over Dupenloup in view of Srinivasan (US 6,701,506), Applicant respectfully traverses the rejections for the record at least for the reason that Dupenloup fails describe each and every limitation recited in the rejected claims 1 and 3, and that Dupenloup and Srinivasan, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims 2 and 4-5.

As amended, claim 1 now recite all of the features of claim 2. As acknowledged by the Examiner in the obviousness rejection of claim 2 in Section 8 in the paragraph bridging pages 4 and 5 of the Office Action, Dupenloup fails to teach specific layout design steps. More specifically, Dupenloup fails to teach Applicant's claimed fifth, sixth and seventh steps.

To cure the deficiencies of Dupenloup, the Examiner relies on Srinivasan as allegedly describing a step for generating the clocks different in the delay amount for the verification of a layout design, a step for step for adjusting skews for each of said clocks, a step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, and step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation, wherein the layout adjustment is repeated according to the constraint violation, as recited in Applicant's claim 2.

In response, Applicant respectfully asserts that Srinivasan's method for match delay buffer insertion is directed to an electrical design (i.e., circuit design), as discussed in numerous portions of Srinivasan. For example, the abstract, the summary of the invention in

col. 4, lines 35-37, and in the detailed description of the preferred embodiments in col. 5, lines 39 of Srinivasan disclose an electrical design. Claim 1 of Srinivasan clearly directs to a method for inserting a delay in a node in an electrical design. That is, the embodiments for inserting a delay in a node an electrical design of Srinivasan is not related to a layout design steps recited in claim 2 of the present invention, and Srinivasan does not teach, disclose, or suggest the steps recited in Applicant's claim 2 directed to layout design steps.

Moreover, the Examiner cited Figs. 1, 5, 6, 7, and 11 of Srinivasan as allegedly showing features corresponding to Applicant's layout design steps. However, when the disclosure of Srinivasan is taken as a whole and in proper context, the method is not directed to a layout design method but to an electrical (i.e., circuit) design. As such, Applicant respectfully submits that Srinivasan does not cure the above-mentioned deficiencies of Dupenloup because Srinivasan does not teach, disclose, or suggest at least fifth, sixth and seventh steps recited in claim 2 or now amended claim 1 of the present invention.

In view of the amendment and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of the §102(b) and §103(a) rejections.

2. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1 and 3-5 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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